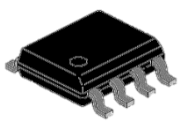
SQ7101/SQ7103
Brief Datasheet V2.1

SQ7101/SQ7103 , Secure ASIC, AES-128/AES-256, SHA-256,TRNG

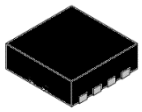
◆ Basic Information

- Operating Voltage : 2.0V ~ 5.5V
- Operating Temperature : -40℃ ~ 85℃

Package Type



SOP8



8-Lead DFN
(3mm x 3mm)

◆ Communication

- SQ7101 support I2C interface (max. 400Kbps)
- SQ7103 support SPI interface (max. 5MHz@MODE 0)

◆ High-Security Features

- AES-128/AES-256
- SHA-256
- True Random Number Generator (TRNG)
- Inclosure Intrusion Protection
- Simple/Differential Power Analysis (SPA/DPA)
- Individual Internal Clock to Prevent Glitch Attack
- 128-bit Unique ID
- NIST CAVP Certification

- Support 16 keys with128-bit or 8 keys with 256-bit
- 256 Bytes User Data
- 768 Bytes Small Zone
- 16 Monotonic Counters, Prevent replay attacks and man-in-the-middle attacks
- Low Power
  - Deep Sleep Current 250nA
- Applications
  - Accessory Authentication
  - System Anti-Clone
  - Security Smart Lock
  - Session Key Exchange
  - Chain of Trust
  - Device Authentication
  - Sensative Data Protection and Encryption
  - Firmware Protection

Content

1. Preface

SQ7101/SQ7103 is high-security, low-power Secure ASIC. This device offers TRNG (True Random Number Generator), Hardware Cryptography AES-128, AES-256, SHA-256 and Anti-Tamper function. The device can support 16 keys with 128-bit or 8 keys with 256-bit.

SQ7101/SQ7103 Secure ASIC is suitable for security application, such as Accessory Authentication, System Anti-Clone, Security Smart Lock, Critical Data Encryption, and so on.

2. Pin Assignment/ Description

2.1 SQ7101 Assignment / Description

PRODUCT : SQ7101SP008C00R

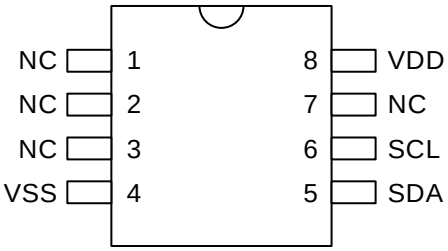


Figure 2-1 Pin Assignment of SQ7101 SOP8

PRODUCT : SQ7101N3008C00R

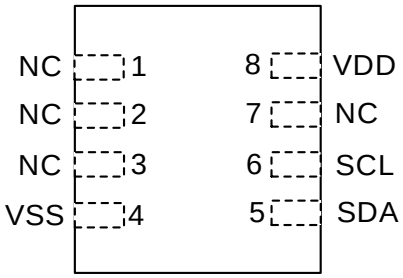


Figure 2-2 Pin Assignment of SQ7101 8-Lead DFN

Pin No.	Pin Name/Pin Option	I/O Type	Function Description
1	NC	-	No Connect
2	NC	-	No Connect
3	NC	-	No Connect
4	VSS	GND	Ground
5	SDA	I/O	SDA, I2C bus data input/output
6	SCL	I	SCL, I2C bus clock input/output
7	NC	-	No Connect

8	VDD	Power	VDD Power Supply

2.2 SQ7103 Assignment / Description

PRODUCT : SQ7103SP008S00R

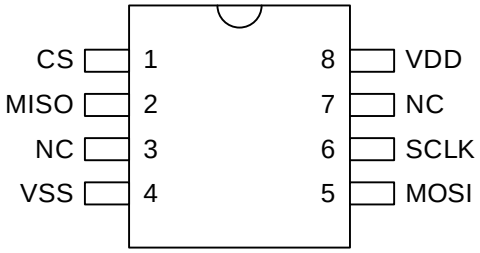


Figure 2-3 Pin Assignment of SQ7103 SOP8

PRODUCT : SQ7103N3008S00R

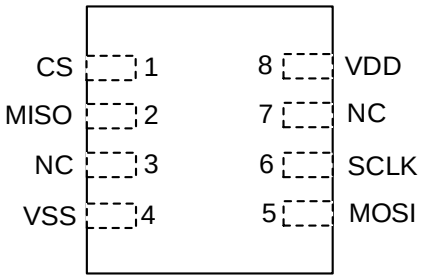
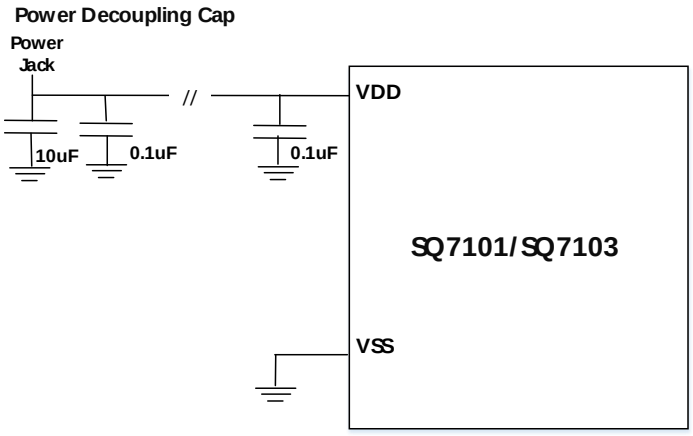


Figure 2-4 Pin Assignment of SQ7103 8-Lead-DFN

Pin No.	Pin Name/Pin Option	I/O Type	Function Description
1	CS	I	SPI, Chip Select
2	MISO	O	SPI, Master In Slave Out
3	NC	-	No Connect
4	VSS	GND	Ground
5	MOSI	I	SPI,Master Out Slave In
6	SCLK	I	SPI,SPI Clock
7	NC	-	No Connect
8	VDD	Power	VDD Power Supply

The following are the recommended reference designs when using SQ7101/SQ7103 products. If the relevant pin are used, please refer to the corresponding suggestions:



Note: The 0.1uF near the IC (VDD) in the above figure should be as close to the IC as possible

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings are rated values which must not be exceeded during operation, even for
an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a
device may break down or its performance may be degraded, causing it to catch fire or explode resulting
in injury to the user. Thus, when designing products which include this device, ensure that no absolute
maximum rating value will ever be exceeded

(V_{SS} = 0V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		-0.3 to 6.0	V
Input Voltage	V_{IN}	All I/O pins	-0.3 to VDD+0.3V	V
Output Current (total)	I_{OL}	All I/O pins	50	mA
Storage Temperature	T_{STG}		-50 to 125	℃

3.2 Operation Conditions

The following defines the electrical characteristics of the device when it is operated at voltage and
temperature maximum/minimum values. Unless otherwise stated, the standard conditions were
determined at "operating temperature 25 ° C and operating voltage VDD = 3.3 V".

3.2.1 Operation Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	2.0	3.3	5.5	V
Operating Temperature	Ta	-40	25	85	℃

3.2.2 I/O Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}		0		0.3 VDD	V
Input HighVoltage	V_{IH}		0.7 VDD		VDD	V
Output Low Voltage	V_{OL}	IOL= 3 mA	0		0.1 VDD	V
Output High Voltage	V_{OH}	IOH= -3 mA	0.9VDD		VDD	V

3.3 DC Characteristics

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Operation Mode	I_{DD_N1}	VDD=3.3V, Temp=25 °C		3		mA
Deep Sleep Mode	I_{DD_DS}	VDD=3.3V, Temp=25 °C		250		nA

3.4 Power-on Reset Characteristics

Ta=-40~85℃

Symbol	Description	MIn	Typ	Max	Unit
tPPW	Power-on reset minimum pulse width	1	-	-	ms
tPWUP	Warming-up time after a reset is clear and device ready	-	4	-	ms
tVDD	Power supply rise time	0.5		5	ms

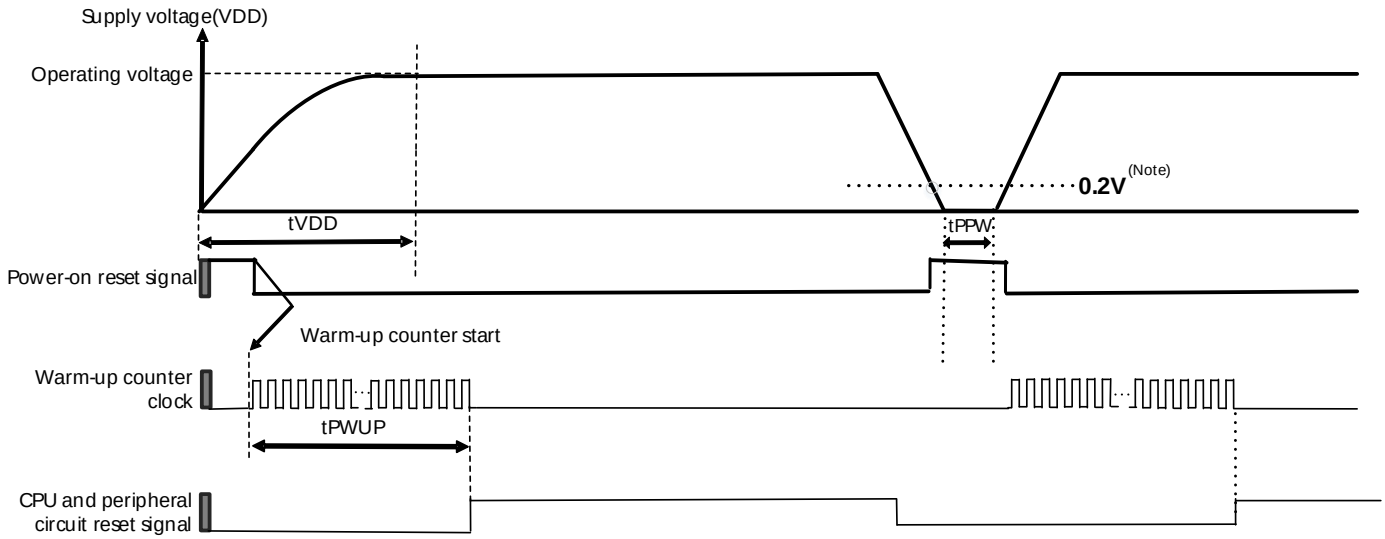


FIGURE 3- 1 OPERATION TIMING OF POWER-ON RESET

Note : In power-down process, the VDD must be less than 0.2V, then re-power-on to ensure the IC operating normal.

3.5 BROR Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Mln	Typ	Max	Unit
BROR detect voltage	VBROR_Rising	VDD rise time and fall time > tVDD (tVDD refer to CH3.4 Power-on Reset Characteristics)	1.95	2.0	2.05	V
	VBROR_Falling		1.85	1.90	1.95	V

3.6 AC Characteristics

Parameter	Symbol	MIn	Typ	Max	Unit
User Data Write Cycle Time (Note)	T_{WC1}	6.0	-	9.0	mS
128-bit/256-bit Key Write Time (Note)	T_{WC2}	6.0		9.0	mS

Note: Writer time is including data update.

3.6.1 AC Parameters

Parameter	Symbol	MIn	Typ	Max	Unit
Power-Up Ready Time	T_{PU_RDY}		2800	9300	uS
Standby Time, Entering deep sleep mode	T_{STB}		55	90	uS
Wake-Up Ready Time, deep sleep mode	T_{WDS_RDY}		300	-	uS

Note : The typ value is under operating temperature 25 ° C and the Sleep command changes this value.

3.6.2 I2C Characteristics

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	0	400	kHz
Hold Time Repeated START Condition	$t_{HD;STA}$	0.6	-	us
Low Period of SCL Clock	t_{LOW}	1.3	-	us
High Period of SCL Clock	t_{HIGH}	0.6	-	us
Setup Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	us
Data Hold Time	$t_{HD;DAT}$	0	0.8	us
Data Setup Time	$t_{SU;DAT}$	0.1	-	us
Rise time of both SDA and SCL	t_r	20	300	ns
Fall Time of both SDA and SCL	t_f	20	300	ns
Setup Time of STOP Condition	$t_{SU;STO}$	0.6	-	us
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	us
Capacitive Load for Each Bus line	C_b	-	400	pF
Note: Guaranteed by characteristic, not tested in production.				

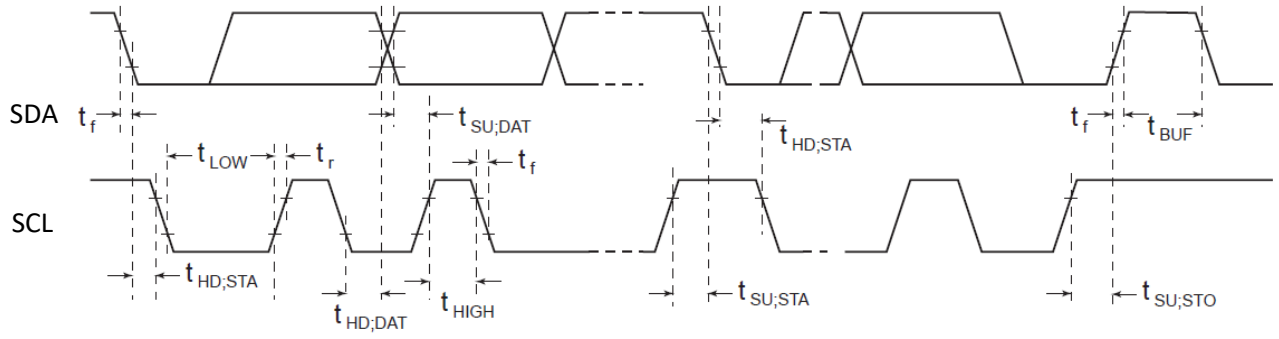


Figure 3-2 I2C Timing Sequence

3.6.3 SPI Characteristics

Parameter	Symbol	MIn	Max	Unit
SPI Frequency	f_{SPI}		5	MHz
SPI Period	t_{SPI}	200		ns
High period of the SCLK pin	t_{CLKH}	90		ns
Low period of the SCLK pin	t_{CLKL}	90		ns
From SPICS active to first edge	t_{CS_SU}	40		ns
From last SCLK edge to SPICS inactive	t_{CS_HD}	40		ns
Time between SPI transaction	t_{CS_WA}	1		us
Data Input Setup Time	t_{SI_SU}	10		ns
Data Input Hold time	t_{SI_HD}	10		ns
Data Output Valid Time	t_{SO_VD}		80	ns
Data Output Hold Time	t_{SO_HD}	0		ns

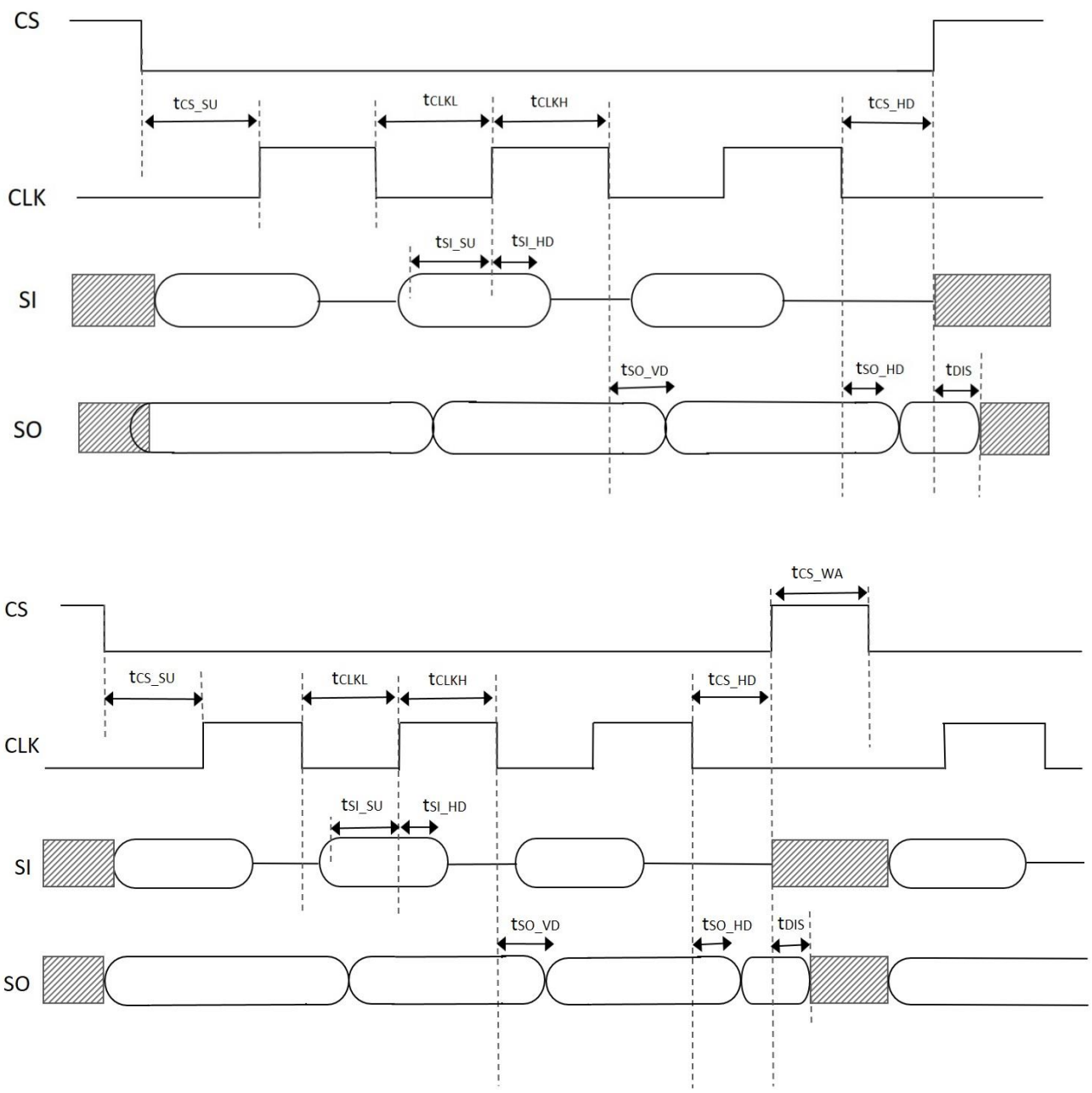


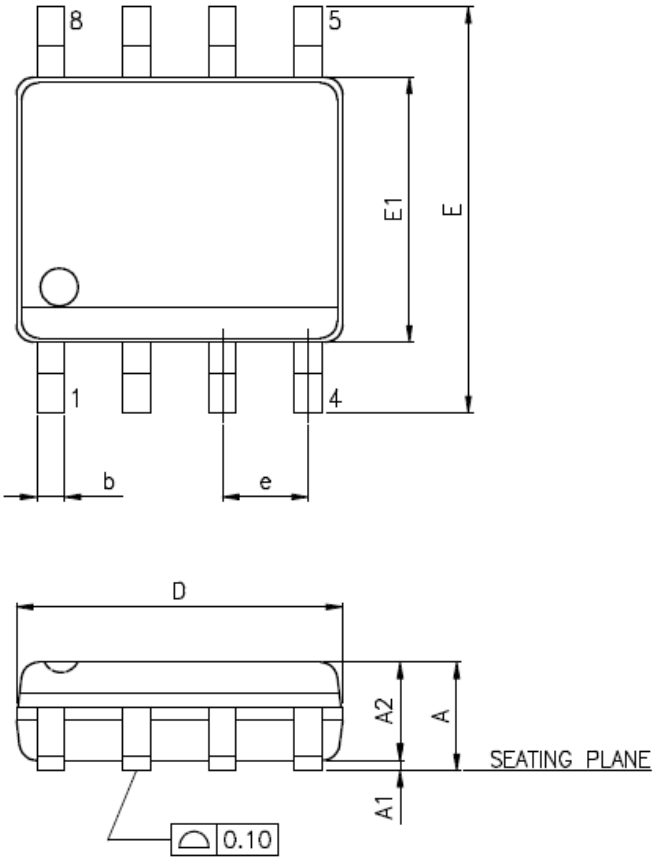
Figure 3-3 SPI Sequence

3.7 EEPROM Characteristics

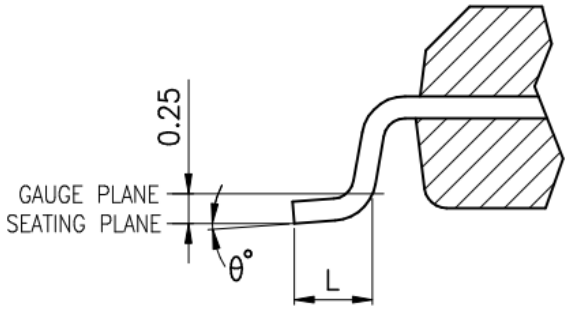
Parameter	Mln	Typ	Max	Unit
Write Endurance (Sector Endurance)	100,000	-	-	Cycles
Data Retention(at 25℃)	100	-	-	Years
Data Retention(at 85℃)	20	-	-	Years

Appendix A. Package Information

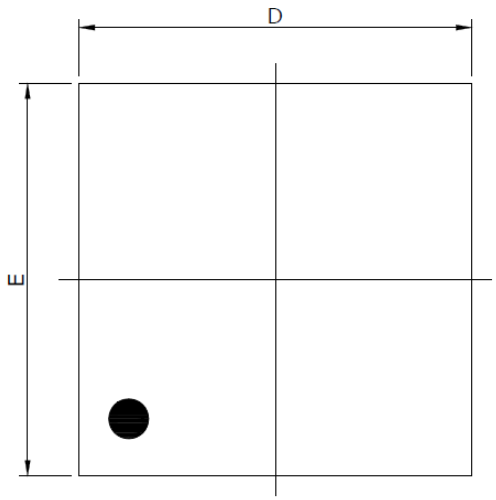
SOP8



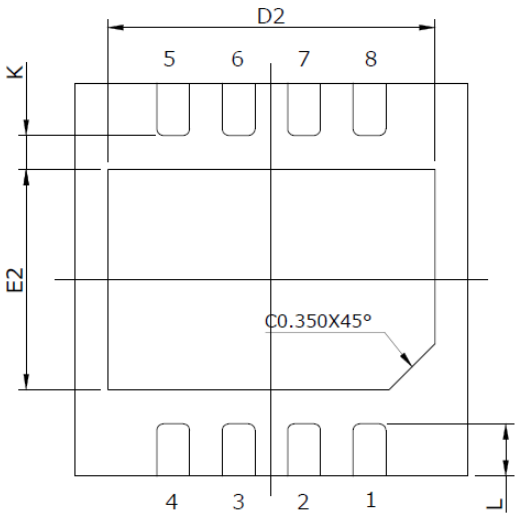
Symbol	mm		
	Min.	Typ.	Max.
A	--	--	1.75
A1	0.10	--	0.25
A2	1.25	--	--
b	0.31	--	0.51
c	0.10	--	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	--	1.27
h	0.25	--	0.50
θ	0°	--	8°



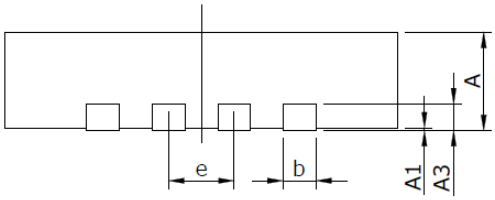
8L DFN (3mm x 3mm)



TOP VIEW



BOTTOM VIEW



Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.50 BSC		
L	0.35	0.40	0.45
D2	2.45	2.50	2.55
E2	1.63	1.68	1.73
K	0.20	--	--

Revision History

Version	Issued Date	Description
V2.1		1. Sync with datasheet V2.1 full version 2. Modify “Supply Voltage” to “Operating Voltage” in 3.2.1 Operation Conditions
V2.0	2024/03/4	3. Sync with datasheet V2.0 full version
V1.9	2023/12/26	1. Sync with datasheet V1.9 full version 2. Add SQ7103 8-Lead DFN package and pin assignment 3. Add PRODUCT info : SQ7101SP008C00R, SQ7101N3008C00R, SQ7103SP008S00R, SQ7103N3008S00R
V1.7	2023/4/20	1. Operating voltage change to 2.0~5.5V, modify “2.1 Absolute Maximum Ratings.” And “2.2.1 Operation Conditions.” 2. Update “figure 2-1 Operation Timing of power-on reset” and add note. 3. “2.6.1 AC Paramenters “add note“Power-Up Ready Time does not include the executing time for BOOTROM code. The BOOTROM code executing time is around 10ms. 4. “3.6.2 I2C Characteristics “ update the figure of $t_{HD;DAT}$ 5. Add SDA and SCL to “figure 2-2 I2C Timing Sequence.”
V1.6	2023/3/30	1.Modify “CH Power-on Reset Characteristics”
V1.5	2022/7/21	1.Modify the description of small zone 2.Add package type “8L DFN 3x3 “ to “1.1 pin assignment/description” and “Appendix A
V1.4	2021/12/29	1.Modify “2.4 Power-on Reset Characteristics” 2.Add ” CH2.5. BROR Characteristics”
V1.3	2021/6/24	1.Solve DecRead issue that Param2 of command is not matched with FirstBlock.Param2. 2. Add : “4.2 SQ7103 Pin Assignment/ Description 3. Add : “5.4.3 SPI Characteristics” 4. Add “ CH5.5 EEPROM Characteristics” description. 5.Add “ CH 7.1 Command Introduction” description. 6. Add “CH 7.3.13 INFO Command “selector for CountStatus. 7. Renew “CH7.3.25 SHA Input Parameters” Mode 8. Add “Appendix A. Package Information”